WHAT IS CLAIMED IS

1. A multi-state memory comprising:

a plurality of EEPROM memory cells, each for storing one of a plurality of multi-states, organized into a plurality of sectors;

one or more tracking cells for each of said multi-states, associated with each of said plurality of sectors;

read circuitry for reading raw data associated with the programmed state of said tracking cells;

converter circuitry for converting said raw data to digital form; and

a memory controller for establishing desired read points for each of a plurality of physical states, based upon said raw data converted to digital form read from each said tracking cell.

2. A multi-state memory comprising:

a plurality of EEPROM memory cells, each for storing one of a plurality of multi-states, organized into a plurality of sectors, each sector comprising an array of rows and columns;

cell operating circuitry comprising:

sense circuitry organized in a column oriented manner;

steering elements organized in a column oriented manner; and

select circuitry organized in a row oriented manner,

wherein one or more selected cells along a row are capable of being read simultaneously;

a reference source;

verification circuitry for selected cells for applying to associated steering elements of said selected cells conditions corresponding to verification of corresponding write state and for receiving read data using said reference source for determining if a selected one of said memory cells has been adequately programmed to the conduction characteristics associated with a desired programmed state; and

write circuitry organized in a column oriented manner,

wherein a selected one or more of said memory cells are capable of being written simultaneously with associated steering elements set to corresponding write states, and including termination circuitry for terminating the programming of selected memory cells along said row being programmed when said verification circuitry indicates said selected memory cells have been adequately programmed to their desired states.

3. A memory as in claim 2 wherein said reference comprises an adjustable reference capable of presenting a plurality of reference values, each associated with one of said multi-states.

4. A memory as in claim 3 wherein said reference comprises a stairstep current source.

5. A memory as in claim 2 wherein said reference comprises a plurality of reference values, each associated with one of said multi-states.

6. A memory as in claim 5 wherein each of said reference values comprises a current source.

7. A memory as in claims 3 or 5 wherein said write circuitry operates to write a selected set of cells along a selected row, independently terminating said programming of each of said selected set of cells when said verification circuitry indicates that level of programming has been achieved.

8. A memory as in claim 2 further comprising a memory controller for establishing desired read points for each of a plurality of physical states, based upon said raw data converted to digital form read from each said tracking cell.

9. A memory as in claims 1 or 8 wherein a sector is the smallest erasable unit.

10. A memory as in claims 1 or 8 wherein said memory controller also determines a physical to logical state translation of each sector.

11. A memory as in claims 1 or 8 wherein said memory controller also determines the quality of data read from each cell.

12. A memory as in claims 1 or 8 wherein said tracking cells are read periodically to establish said read compare points.

13. A multi-state memory as in claim 12 wherein said tracking cells are read in the event of a failure in order to establish said read compare points.

14. A memory as in claims 1 or 8 wherein said tracking cells are read as part of normal read operations in order to reestablish said read compare points.

15. A memory as in claims 1 or 8 wherein said raw data comprises memory cell current measurements.

16. A memory as in claims 1 or 8 wherein said compare points are established with an optimum margin established based upon the raw data read from said tracking cells.

17. A memory as in claims 1 or 8 wherein said memory controller also establishes poor margin compare points.

18. A multi-state memory as in claim 17 wherein said poor margin compare points are used to provide a measure of the quality of data read from memory cells.

19. A multi-state memory as in claim 18 wherein said memory controller, in response to determining that read data has poor margin, causes said data to be rewritten.

20. A multi-state memory as in claim 19 wherein said rewriting of data is performed on a cell basis if the poor margin read data requires a cell to be moved to a more programmed state.

21. A multi-state memory as in claim 19 wherein said rewriting of data is performed on a sector basis if the poor margin read data requires a cell to be moved to a less programmed state.

22. A multi-state memory as in claim 21 wherein said reprogramming is performed by erasing the sector, and then reprogramming the sector.

23. A memory as in claim 19 which further comprises a counter for maintaining a count of the number of times data is rewritten in response to poor margin and, upon reaching a predetermined count, causes selected ones of said memory cells to be mapped out rather than rewritten.

24. A memory as in claim 23 which comprises one such counter per sector.

25. A memory as in claims 1 or 8 wherein said memory cells and said memory controller are contained on a single integrated circuit.

26. A memory as in claims 1 or 8 wherein said memory cells are contained in one or more integrated circuits, and said memory controller is contained on another integrated circuit.

27. A memory cell comprising:

a read/write path;

a read only path; and

a floating gate common to said read/write and said read only paths.

28. A memory cell as in claim 27 wherein both said read/write and said read only paths are used during reading.

29. A memory comprising:

a plurality of EEPROM memory cells organized into a plurality of sectors, each sector including at least one wear detecting cell comprising:

a read/write path;

a read only path; and

a floating gate common to said read/write and said read only paths; and

control circuitry for detecting the difference in conduction characteristics of said read/write and read only paths during reading, to measure the amount of wear of said wear detecting cell.

30. A memory as in claim 29 which further comprises:

replacement sectors for replacing those ones of said sectors having associated wear detecting cells which exhibit excessive wear.

31. A memory as in claim 29 wherein said control circuitry causes both said read/write and said read only paths to be operated during each reading of a memory cell.

32. A memory as in claim 29 wherein said control circuitry causes both said read/write and said read only paths to be periodically operated.

33. A memory as in claim 32 wherein both said read/write and said read only paths are operated based on one or more of the following events: data read failure, data read poor marginality, passage of time, number of read cycles, number of write cycles, and number of erase cycles.

34. A memory as in claim 32 wherein both said read/write and said read only paths are operated based on a random number generator.

35. A method of operating a memory which comprises a plurality of word lines, and a plurality of EEPROM memory cells, each cell uniquely associated with one word line and one bit line, each memory cell having a floating gate electrode, a

steering electrode, and an erase electrode, said method comprising the steps of:

selecting one or more of said memory cells along a row;

controlling the magnitude of a steering voltage applied to said steering electrodes of said selected one or more memory cells, on a cell by cell basis;

establishing erase potentials on said selected one or more memory cells, thereby removing charge from said floating gates of said selected one or more memory cells,

wherein the magnitude of electron removal from each floating gate is established on a cell by cell basis by the magnitude of the steering potential applied to its associated steering electrode.

36. A method as in claim 35 which further comprises the steps of iteratively:

pulsing said erase potentials;

determining which cells have been adequately erased; and

again pulsing said erase potentials for those cells which have not been adequately erased and terminating application of said erase potentials on cells which have been adequately erased.

37. A method as in claims 35 or 36 wherein said erasure serves to write data to said selected memory cells.

38. A method as in claim 37 wherein said data is represented by less or equal charge on said floating gates than the amount of charge on said floating gates prior to said erasure.

39. A method as in claim 38 wherein said data comprises multi-state data.

40. A method as in claim 38 wherein establishing said amount of charge on said floating gates prior to said erasure is accomplished by hot electron programming from a source region of said memory cell to said floating gate of said memory cell.

41. A method as in claim 35 which further comprises the steps of:

dividing said word line of memory cells into a plurality of subsets of memory cells;

simultaneously erasing each of said subsets of memory cells; and

terminating the erasure of each of said subsets of memory cells on a cell by cell basis when all memory cells in a given subset have been adequately erased, regardless of whether erasure of others of said subsets of memory cells has been completed.